--This application is a continuation of application serial no. 09/395,873, entitled "Design Verification by Symobolic Simulation Using a Native Hardware Description Language," filed September 14, 1999 and assigned to the corporate assignee of the present invention.--

IN THE CLAIMS

Please cancel claims 5 and 15.

Please amend the following claims.

1. (Currently Amended) A method for performing design verification, the method comprising:

specifying at least one description language object that represents at least one signal as a symbol in a design using a first statement that is part of a description language ~~programming interface call (PLI) command~~; and

instructing a symbolic simulator in response to the first statement ~~with the first command~~ to treat the at least one description language object as a symbol.

2. (Currently Amended) The method defined in Claim 1 further comprising:

inserting the first statement ~~command~~ into a design specification; and

inputting the design specification into the symbolic simulator.

3. (Currently Amended) The method defined in Claim 1 wherein the at least one description language object comprise a hardware description language object.

4. (Currently Amended) The method defined in Claim 1 wherein the at least one description language object comprises a Verilog object.

5. (canceled)

6. The method defined in Claim 1 wherein the at least one signal comprises an input.

7. (Currently Amended) The method defined in Claim 1 further comprising:

specifying a check using a second statement ~~command~~, the check to perform a test to validate design functionality; and

instructing the symbolic simulator using the second statement ~~command~~ to perform the test.

8. (Currently Amended) The method defined in Claim 7 further comprising:

inserting the first and second statements ~~commands~~ into a design specification; and

inputting the design specification into the symbolic simulator.

9. (Currently Amended) The method defined in Claim 7 wherein the second statement ~~command~~ comprises a PLI.

10. The method defined in Claim 7 further comprising:

instructing the symbolic simulator to generate a file with information to locate an identified fault.

11. (Currently Amended) An article of manufacture having at least one recordable medium having stored thereon executable instructions which, when executed by at least one processing device, cause the at least one processing device to:

specify at least one description language object that represents at least one signal as a symbol in a design using a first statement that is part of a design language ~~command~~; and

instruct a symbolic simulator in response to the first statement ~~with the first command~~ to treat the at least one description language object as a symbol.

12. (Currently Amended) The article of manufacture defined in Claim 11 further comprising executable instructions stored on the at least one recordable medium which, when executed by at least one processing device, cause the at least one processing device to:

insert the first statement ~~command~~ into a design specification; and

input the design specification into the symbolic simulator.

13. (Currently Amended) The article of manufacture defined in Claim 11 wherein the at least one description language object comprise a hardware description language object.

14. (Currently Amended) The article of manufacture defined in Claim 11 wherein the at least one description language object comprises a Verilog object.

15. (Canceled)

16. The article of manufacture defined in Claim 11 wherein the at least one signal comprises an input.

17. (Currently Amended) The article of manufacture defined in Claim 11 further comprising executable instructions stored on the at least one recordable medium which, when executed by at least one processing device, cause the at least one processing device to:

specify a check using a second statement ~~command~~, the check to perform a test to validate design functionality; and

instruct the symbolic simulator using the second statement ~~command~~ to perform the test.

18. (Currently Amended) The article of manufacture defined in Claim 17 further comprising executable instructions stored on the at least one recordable medium which, when executed by at least one processing device, cause the at least one processing device to:

insert the first and second statements ~~commands~~ into a design specification; and

input the design specification into the symbolic simulator.

19. (Currently Amended) The article of manufacture defined in Claim 17 wherein the second statement ~~command~~ comprises a PLI.